Design Considerations For Large Area Professional DSC CCD Imager Output Amplifiers

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Abstract

In this paper, we present the design considerations for an new amplifier that suits the needs for large area CCD's for Digital Still Camera applications. A 3D off state device simulator supported the improvement process by performing extended capacitance calculations with about 1 million mesh points. The improvement with respect to readout noise and conversion factor measured on silicon resembled the predicted values of the simulation within a 10% margin.
By using a specific mask layout and the 'stitching' principle the several amplifier prototypes could be evaluated at once and directly on the imager.

Introduction

The market for large area Charged Coupled Device (CCD) Imagers for the professional Digital Still Camera (DSC) applications persistently demands higher pixel counts on the widely accepted formats like the 35 mm [1] and 645 format. Consequently, smaller pixels will be applied, resulting in an intrinsic lower performance on sensitivity. This lower performance should be compensated both by improving quantum efficiency and by improving the conversion factor of the amplifier. Although improving the Quantum Efficiency, as described earlier [2], is for some applications or modes of operation more advantageous than improving the conversion factor, the latter is still required because of readout noise considerations, especially at moderate illumination and integration times (region II in figure 1). An amplifier with a higher conversion has an intrinsically lower input capacitance and, when properly designed, also a lower parasitic capacitance and therewith on the whole a lower amplifier or readout noise [5]. For certain applications of the 35mm and 645 format CCD with 9µm square pixels, an amplifier is required, which is capable of handling a charge packet of 100 kel, has a bandwidth exceeding 85 MHz, a conversion factor of 20 µV/el and noise lower than 1.4 el/√MHz. This is a challenging target to achieve in the currently used and yield-friendly three-poly single-metal process. A new approach is using 3D off state capacitance simulations to evaluate different design options with respect to optimising the input capacitance. A special mask layout and the use of 'stitching' technique enabled the prototyping of 10 different amplifiers at once. These different designs have resulted in many alternatives for other applications. Also requirements for new process options have been deducted from the capacitance simulations, to support the new design features that enable an increase of the conversion factor and a reduction of the noise.

Simulations

The use of a 3D off-state device simulator made it possible to obtain insight in the crucial capacitance contributions, responsible for both the useful and non-useful or parasitic capacitance. This proprietary device simulator is able to calculate device structures (see figure 2) built up from more than 1 million grid points and run it within 10 to 15 minutes (see also [3]). This enabled multiple complex calculations of very different configurations and gave valuable design information. Basically, the simulator calculates the charge distribution at standard operating conditions, which is compared with the calculated charge distribution after one specific terminal is slightly altered; e.g. +0.1 V on the Floating Diffusion (FD) terminal. The difference, i.e. ΔQ in the other isolated terminals, together with the ΔV, gives the capacitance of this terminal towards the other. The main factors of interest with respect to minimizing parasitic capacitance could be identified and

taken into account during the design. The main areas of concern are the Drain-Gate capacitance of Source Follower One (SF1), the Floating Diffusion-Output Gate capacitance and the interconnect between the gate and Floating diffusion (see table 1). Although the Source-Gate capacitance is higher then the Drain-Gate capacitance, it is less important for the conversion factor because the source 'follows' the gate and reduces this capacitance with a factor of typical $(1-A_{DC})$, with A_{DC} the DC gain of the first stage. The simulated conversion factor and noise matches the measurements of the silicon within 10%. With the results of the 3D simulator, the FD and SF1 were designed in such a way that the functionality was still maintained, while the parasitic capacitance was minimized.

Mask design, Output Amplifier Architecture and Process options

The modular 'stitching' design, like the concept described in [4], enables a flexible system in which several amplifier prototypes can be evaluated and tested on-chip as a complete imager. The masks for the subsequent layers contain, besides other building blocks, ten amplifier blocks, each with different concepts or features (see figure 3). After evaluation and selecting the 'winning' design for this specific application, only a change of the stepper litho program is sufficient to take the sensor with the new amplifier concept into production. This makes prototyping very efficient and therewith increases the innovation speed. It also enables tailor-made CCD solutions very efficiently, in which one of the alternative amplifiers can be applied for specific applications. The architecture is a commonly used three-stage source follower, with, for this technology uncommon use of surface MOSFET's for both SF1 and the Reset FET. Although surface FET's have intrinsically higher noise figures than buried FETs with the same size [5], the overall noise performance of surface FET designs is better. This because the length and to some extent the width can be reduced, without risk of 'short channel' effects caused by the out diffusion of source and drain implants in combination with the buried channel. With respect to bandwidth, a surface FET performs better than a buried FET. Basically, the sensor is designed in a three-poly gate, single-metal process [1]. However, in order to reduce the parasitic capacitance of the interconnect, an intermediate metal is added to the existing technology. With this tungsten metal it is possible to construct very small contact holes compared to the commonly used aluminium contact holes (see figure 4) and therewith reducing the parasitic capacitance.

Performance of the new amplifier.

The 'winning' amplifier has excellent results. The conversion factor is nearly doubled from 11µV/el to 21µV/el and the noise is reduced from 1.4 el/√MHz to 1.1 el/√MHz. The bandwidth is 100 MHz, which is more than sufficient for 25 MHz readout (see figure 5). The power dissipation remains under 76 mW and the amplifier is capable of handling a 100 kel charge packet with better than 99% linearity. This results in a 2V max output voltage, still matching with the input range of the Front-End IC.

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[1] J.Bosiers et al. "A35mm Format 11M Pixel Full-Frame CCD for Professional Digital Still Imaging", IEEE Transactions on Electronic Devices, vol. 50, No.1 January 2003

[2] C.Draijer et al. "A Color Image Sensor with 9µm Pixels for High-End Digital Still Photography", 2001 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors.

[3] A.Heringa et al., "Automated optimisation of FT-CCD Image Pixels", 1997 IEEE Workshop on Charge Coupled Devices and Advanced Image Sensors.

[4] G.Kreider, J.Bosiers, "An mKxnK Bouwblok CCD image sensor family"; part 1 & 2, IEEE Trans. Electron Devices, vol. 59, pp316-376.

[5] P.Centen, E.Roks, "Characterization of Surface- and Buried Channel Detection Transistors for On-Chip Amplifiers", IEDM Technical Digest, pp. 193-196, Dec 1997

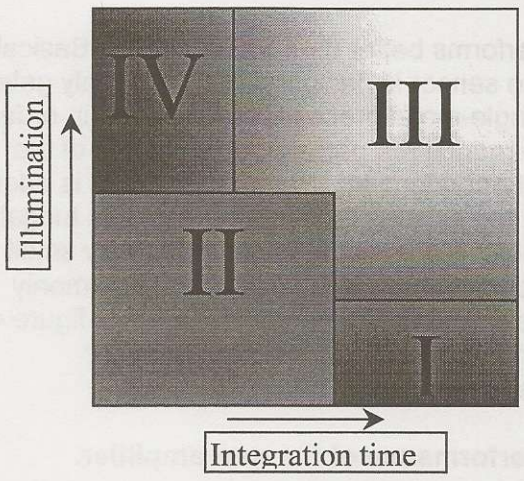

Figure 1: A schematic representation of the dominant noise regimes. In regime I, the dark current is dominant, in regime II, at the origin, the readout noise is dominant. In regime IV, the photon shot noise is dominant, while elsewhere (III) the photon shot noise duals with the dark current shot noise.

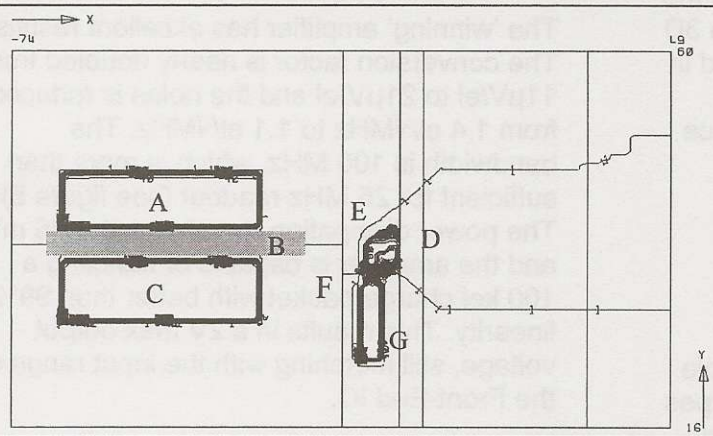

Figure 2: An overview of the input structure of the 3D simulator; A is the drain area, B the gate area, C the source area, D the Output Gate area, E the Floating Diffusion, F the Reset FET gate area and G the Reset Drain area

Tabel 1: Simulated and measured noise values

Quantity	*Symbol*	*Unit*	*Simulated results*	*Measured results on Silicon*
Drain-Gate Capacitance	A	F	3.45E-15	-
Source-Gate Capacitance	B	F	9.34E-15	-
Interconnect Capacitance	C	F	1.1E-15	-
Floating Diffusion Capacitance	D	F	9.52E-16	-
Total Capacitance	E	F	1.53E-14	-
Transconductance SF1	F	Ω^{-1}	-	1.05E-4
Transconductance CS1	G	Ω^{-1}	-	5.0E-4
Noise Electron Density	H	el^2/MHz	1.42[1]	1.7
Noise	I	el/√MHz	1.19	1.3
Gain Amplifier	J		-	0.8
Gain SF1	K		-	0.9
Estimated input capacitance SF2	L	F	3.3E-14	-
Effective Source-Gate capacitance	M	F	4.15E-15[2]	-
Total Detection Capacitance	N	F	1.11E-14	1.165E-14[4]
Conversion factor	O	µV/el	11.5[3]	11

(1) $NED = \alpha \frac{4kT}{g_{m1}} \left[1 + \frac{g_{mc}}{g_{m1}} \right] \left[\frac{E}{q} \right]$

(2) (L+B)*(1-K)

(3) $ConversionFactor = \frac{1}{N} \cdot q \cdot J$

4) calculated from the measured Conversion Factor (O)

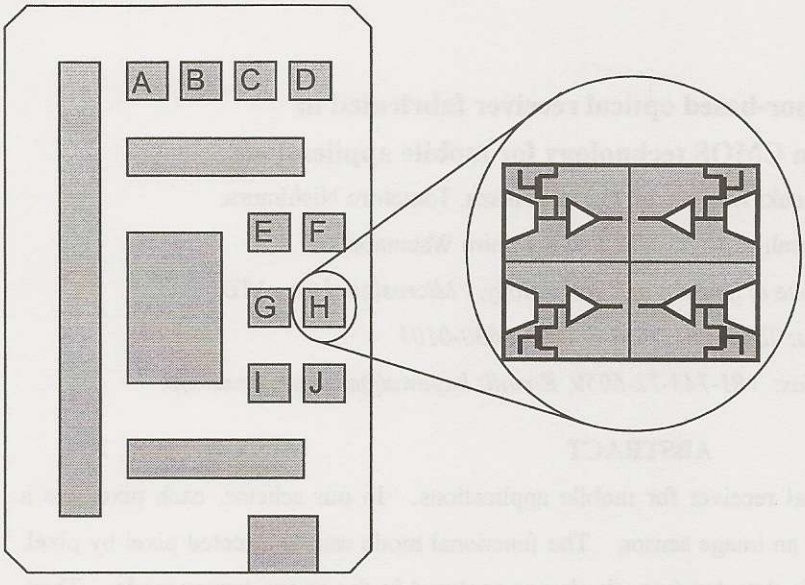

Figure 3: The mask layout (for one layer) that enables the on chip evaluation of ten different amplifier concepts. Every block contains amplifiers at every corner for four adjacent sensors, which will be separated after processing.
For the image area, a separate mask is used.

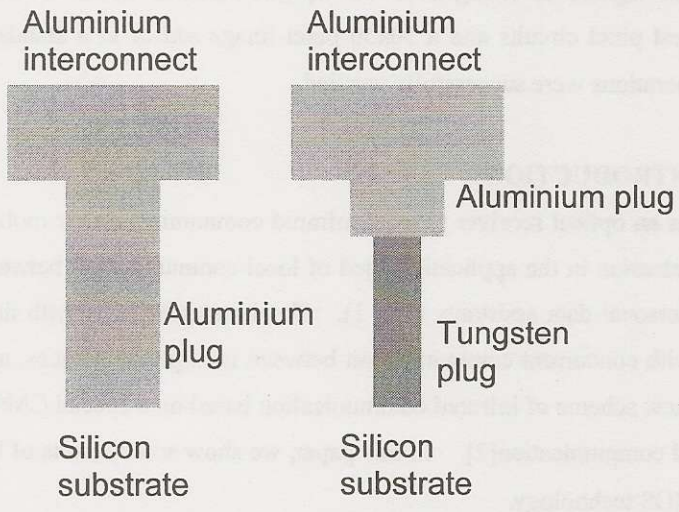

Figure 4: The previous contact to implanted silicon(left) and the modified one (right) in which Tungsten is applied reducing the parasitic capacitance. Both contact holes are also used to contact poly silicon gates.

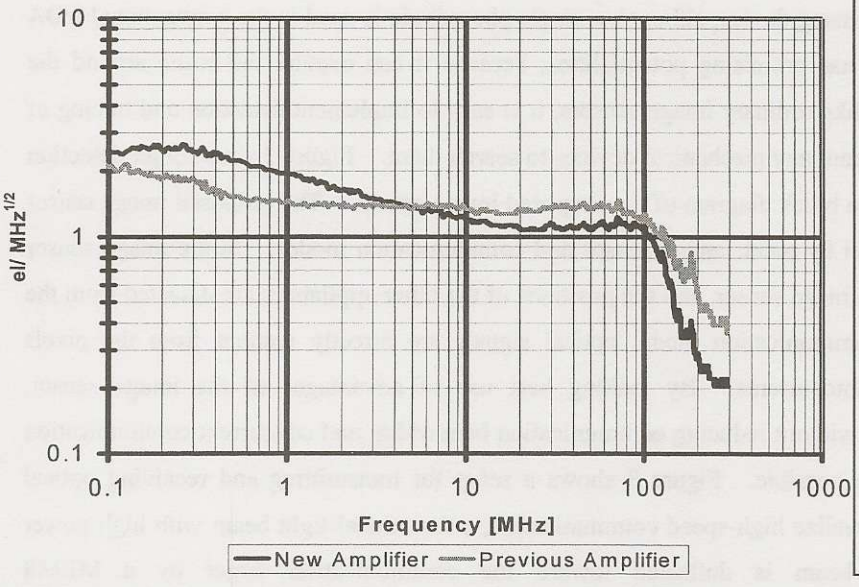

Figure 5: The noise spectra of the previous and new amplifier. The thermal noise is reduced with 25% and the bandwidth is more than sufficient with 100 MHz. The 1/f ramp is more pronounced for the new amplifier which is due to the smaller dimension of the first Source Follower.